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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TAN, VIBOL	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 05/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/804,840	SUH, JUNGWON	
	Examiner	Art Unit	
	Vibol Tan	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 14-31* is/are rejected.

7)☒ Claim(s) *13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/19/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 9-12 and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Ooishi (U. S. PAT. 6,246,614).

In claim 9, Ooishi teaches all claimed features in Fig. 1, a memory comprising: a clock stop detector (5) configured to receive a clock signal (CLK) and output a control signal in response to the clock signal (CKE) and a peripheral circuit (6) for reading and writing data (see Fig. 3) to a memory bank (4), wherein the peripheral circuit is configured to receive the control signal (CKE) and activate and deactivate in response to the control signal (see Fig. 3).

In claim 10, Ooshi further teaches the memory of claim 9, further comprising: a clock receiver (2) configured to receive an external clock signal (CLK) and pass the clock signal to the clock stop detector (5).

In claim 11, Ooshi further teaches the memory of claim 9, further comprising: an address receiver (located inside peripheral circuit 6) configured to receive the control signal (CKE) and activate and deactivate in response to the control signal.

In claim 12, Ooshi further teaches the memory of claim 9, further comprising: a command receiver (Fig. 3) configured to receive the control signal (CKE) and activate and deactivate in response to the control signal.

In claim 16, Ooshi further teaches the memory of claim 9, wherein the memory comprises a random access memory (Fig. 1).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-5, 7, 8 and 20-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over De (U. S. PAT. 5,841,299) in view of Nakashima (U. S. PAT. 5,517,144).

In claim 1, De teaches all claimed features in Fig. 1, a clock stop detector for a memory comprising: a first switch (14) that closes in response to a first logic level (logic 0) of a clock signal (IN) to charge a capacitor (20); a second switch (16) that closes in response to a second logic level (logic 1) of the clock signal to discharge the capacitor; with the exception of teaching a logic circuit that outputs a control signal based on an inverted clock signal and a charge on the capacitor. However, Nakashima teaches in Fig. 2, a logic circuit (16) that outputs a control signal (RESET PULSE) based on an inverted clock signal (output from 18) and a charge on the capacitor (12).

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to combine the teachings of De with the teachings of Nakashima in order to provide a power-on reset circuit that generates a reset signal with stability without affected by a rising characteristic of a power-supply voltage.

In claims 2 and 3, De further teaches the clock stop detector of claim 1, wherein the first switch comprises a first transistor (14) and the second switch comprises a second transistor (16); and wherein the first transistor is a p-type metal-oxide semiconductor field effect transistor (pMOS) and the second transistor is an n-type metal-oxide semiconductor field effect transistor (nMOS).

In claim 4, Nakashima further teaches the clock stop detector of claim 1, wherein the logic circuit comprises a NOR gate (19).

In claims 5, 7 and 8, De further teaches the clock stop detector of claim 1, wherein the first logic level is a logic low logic level (logic 0) and the second logic level is a logic high logic level (1); a power supply voltage (Vcc) coupled to the first switch (14) to charge the capacitor (20) if the first switch is closed (logic 0); and wherein the second switch (16) is open (logic 0) if the first switch is closed and the first switch is open if the second switch is closed.

Claims 20 and 21 correspond to detailed circuitry already discussed similarly with regard to claims 1-5 and 7-8.

Claims 22-28 correspond to detailed circuitry already discussed similarly with regard to claims 1-5 and 7-8.

5. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over De in view of Nakashima as applied to claim 1 above, and further in view of Forbes (U. S. PAT. 6,649,476).

In claim 6, De in view of Nakashima teaches the clock detector of claim 1; with the exception of teaching a current source coupled to the second switch to discharge the capacitor if the second switch is closed. However, Forbes teaches in Fig. 1, a current source (16) coupled to the second switch (20) to discharge the capacitor (not marked) if the second switch is closed.

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to combine the teachings of De in view of Nakashima with the teachings of Forbes in order to provide a power-on reset circuit that generates a reset signal with stability without affected by a rising characteristic of a power-supply voltage.

6. Claim 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ooshi.

In claim 17, Ooshi teaches the memory of claim 9; with the exception of teaching wherein the memory comprises a dynamic random access memory. However, it is obvious to one ordinary skill in the art to select a dynamic random access memory for the memory because the dynamic random access memory equipped with synchronous clock.

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to select a dynamic random access memory for the memory in order to synchronize data during read/write operation.

In claim 18, Ooshi teaches the memory of claim 9; with the exception of teaching wherein the memory comprises a double data rate synchronous dynamic random access memory. However, it is obvious to one ordinary skill in the art to select a double data rate synchronous dynamic random access memory because it operates on both edges of the clock signal; thus high-speed operation can be achieved.

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to select a double data rate synchronous dynamic random access memory for the memory in order to accurately synchronize data during read/write operation with high-speed.

In claim 19, Ooshi teaches the memory of claim 9; with the exception of teaching wherein the memory comprises a mobile random access memory. However, it is obvious to one ordinary skill in the art to select a mobile random memory for memory because mobile random memory requires low power to operate; thus it is suitable for hand-held electronic devices.

7. Claims 14, 15 and 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ooshi in view of De and further in view of Nakashima.

In claim 14, Ooshi teaches the memory of claim 9; with the exception of teaching details of the clock stop detector. However, De in view of Nakashima, as discussed in claim 1, teaches a clock stop detector for a memory comprising: a first switch (14) that

closes in response to a first logic level (logic 0) of a clock signal (IN) to charge a capacitor (20); a second switch (16) that closes in response to a second logic level (logic 1) of the clock signal to discharge the capacitor; and Nakashima teaches in Fig. 2, a logic circuit (16) that outputs a control signal (RESET PULSE) based on an inverted clock signal (output from 18) and a charge on the capacitor (12).

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to combine the teachings of Ooshi with the teachings of De and with the teachings of Nakashima in order to provide a power-on reset circuit that generates a reset signal with stability without affected by a rising characteristic of a power-supply voltage which can be use in a memory device.

In claim 15, De further teaches the memory of claim 14, wherein the first switch comprises a first transistor (14) and the second switch comprises a second transistor (16).

Claims 29 and 30 correspond to detailed circuitry already discussed similarly with regard to claim 14.

8. Claim 31 rejected under 35 U.S.C. 103(a) as being unpatentable over Ooshi in view of De further in view of Nakashima as applied to claim 29 above, and further in view of Choi et al. (U. S. PAT. 6,381,188).

In claim 31, Ooshi in view of De further in view of Nakashima and further in view of Choi et al. teaches the portable device of claim 29; with the exception of teaching wherein the portable electronic device comprises one of a cellular telephone, a personal digital assistant, a music player, a game system, a digital camera, and a computer.

However, Choi et al. teaches in col. 1, lines 33-40, DRAMs installed on recent systems including Pentium-type computer combined personal data assistance systems (PDA).

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to combine all the teachings, as discussed above, in order to implement PDA systems, which commonly operate on battery power, it is necessary to minimize power consumption.

9. Claim 13 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (571) 272-1811. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike J. Tokar can be reached on (571) 272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VIBOL TAN
PRIMARY EXAMINER